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09/727,513	12/04/2000	Sang-Jin Lee	P56254	5550

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EXAMINER	
CHAI, LONGBIT	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,513	LEE, SANG-JIN	
	Examiner	Art Unit	
	Longbit Chai	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. New claims 16 – 21 have been added in an amendment filed 9/23/2004. Claims 1 – 21 have been examined.

Priority

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Korea on December 2, 1999. Therefore, the effective filing date for the subject matter defined in the pending claims in this application is 12/2/1999.

Response to petition

3. Applicant's arguments filed on 3/28/2005 have been fully considered and Examiner's explanations are presented as follows.

4. Applicant argues the grounds of rejection of Final Office action (submitted on January 4, 2005) has been changed by the Examiner with minor errors in two words. Examiner notes the grounds of rejection of Final office action is indeed not changed from "Oka" to "Lay in view of Oka" – This is because the 2nd Non-Final Office action was submitted on June 25/2004 due to the errors of priority date admitted by Examiner (2 weekend days used by Applicant for being just qualified to meet 1-year foreign priority date). However, the Attorney is still referred to the 1st Office action (submitted on June 8/2004), where Oka – 102(b) reference is used instead of 2nd Non-Final Office action (submitted on June 25/2004), where the reference of Lay in view of Oka – 103(a) is used.

5. Applicant argues: "Examiner shifted his position regarding the rationale for rejecting the instruction pointer limitation of claims 10 and 11 from the references of Lay in view of Oka to now saying that the instruction pointer feature is inherent". Examiner notes "setting an instruction pointer of a CPU to a boot image in main memory is deemed a "MUST" in order to successfully execute booting the device. This implicit inherency as stated in my Final Office action (submitted on January 4, 2005) merely intends to further emphasize this inherency in conjunction with the general art rejection cited in the 2nd Non-Final rejection (submitted on June 25/2004).

6. The decision of re-opening of the prosecution with a new Office action is made by Examiner in response to the petition (filed on 3/28/2005) and arguments (filed on 3/28/2005).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 11, 12 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Iga (Patent Number: 6226740).

As per claim 11, Iga teaches a method for booting a computer, comprising the steps of:

providing a central processing unit (CPU) having an instruction pointer and a memory for storing a boot image and a main memory (Iga: see for example, Column 1 Line 45 – 48and Figure 1: an instruction pointer must be embodied with a CPU);

reading out said boot image (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36);

loading said boot image into said main memory (Iga: see for example, Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36);

setting said instruction pointer of said CPU to point to said boot image in main memory; and executing an operating system by reading out said boot image from main memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36: Iga teaches booting is carried out using the content of the cache (i.e. higher speed RAM relative to lower speed ROM storage device), the processor reads out from a contents of high speed RAM instead of the contents of low speed ROM; as a result, this makes it possible to significantly reduce the boot time (Column 4 Line 32 – 36) – Therefore, the instruction pointer must be incorporated into this booting process in order to successfully execute booting the system).

As per claim 12, Iga teaches the claimed invention as described above (see claim 11). Iga further teaches said memory for storing said boot image prior to reading out said boot image being a boot image memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36).

As per claim 21, Iga teaches the claimed invention as described above (see claim 11). Iga further teaches executing step occurring without having to transfer said boot image from said main memory to another location (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36).

8. Claims 7 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Reneris (Patent Number: 5784628).

As per claim 7, Reneris teaches a method for powering down a computer receiving main and auxiliary power, the method comprising the steps of:

providing a central processing unit, a main memory, a basic input/output system memory and a boot image storing device (Reneris: see for example, Column 5 Line 60 – 64);

determining whether the computer is powered down (Reneris: see for example, Figure 4 Element 100 and Column 16 Line 51 and Column 9 Line 42 – 54).

reading out a boot image from the boot image device (Reneris: see for example, Column 16 Line 55 – 56: device / processor state is also qualified as one form of a boot image); and

storing the read boot image to the main memory (Reneris: see for example, Column 16 Line 55 – 56: saving includes reading out and storing in);

supplying the auxiliary power to the main memory (Reneris: see for example, Column 9 Line 46 – 48: turning off the main power switch except the power to memory is maintained and RAM is refreshed); and

shutting off the main power (Reneris: see for example, Column 16 Line 58).

As per claim 18, Reneris teaches the claimed invention as described above (see claim 7). Reneris further teaches said reading, said storing and said supplying steps occurring upon said determination that said computer is being powered down (Reneris: see for example, Figure 4 Element 100, Figure 6 Element 245 and Column 16 Line 51 – 60 and Column 9 Line 42 – 54).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 4, 6, 8, 9, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reneris (Patent Number: 5784628), in view of Iga (Patent Number: 6226740).

As per claim 1, Reneris teaches a computer, comprising:

a central processing unit (Reneris: see for example, Figure 1 Element 12);

a main and/or auxiliary power supply for supplying main and/or auxiliary power of the computer (Reneris: see for example, Figure 6 Element 245 & Column 9 Line 44 – 49 and Column 14 Line 1);

a boot image storing device for storing a boot image of the computer (Reneris: see for example, Column 5 Line 62 – 64);

Reneris teaches saving the device / processor state in any given state into RAM upon powering down the main power supply (Reneris: see for example, Column 16 Line 55 – 56). However, Reneris does not disclose expressly storing the boot image from the boot image storing device into RAM before powering down (i.e. initial state).

Iga teaches:

a main memory for storing the boot image from the boot image storing device by receiving the auxiliary power when the main power is shut off (Iga: see for example, Column 4 Line 16 – 22).

a composition memory for setting an instruction pointer of the central processing unit to a specific region of the main memory storing the boot image, wherein the central processing unit loads the boot image from the specific region of the main memory in response to the instruction pointer, allowing an operating system program to perform control functions (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36: Iga teaches booting is carried out using the content of the cache (i.e. higher speed RAM relative to lower speed ROM storage device), the processor reads out from a contents of high speed RAM instead of the contents of low speed ROM; as a result, this makes it possible to significantly reduce the boot time (Column 4 Line 32 – 36) – Therefore, the instruction pointer must be incorporated into this booting process in order to successfully execute booting the system).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Iga within the system of Reneris because (a) Reneris teaches saving the device / processor state in any given state into RAM upon powering down the main power supply (Reneris: see for example, Column 16 Line 55 – 56) and (b) Iga further teaches an improved low cost and fast reboot mechanism by saving the entire boot image code using the existing RAM before powering down (i.e. initial state) instead of using regular low speed boot ROM to speed up the booting process (Iga: see for example, Column 2 Line 24 – 26).

As per claim 2, Reneris as modified teaches the claimed invention as described above (see claim 1). Reneris further teaches the auxiliary power supply is composed of alternative one of a battery and a suspend voltage supplying unit of the main power supply (Reneris: see for example, Figure 6 Element 245 and Column 14 Line 1).

As per claim 4, Reneris as modified teaches the claimed invention as described above (see claim 1). Iga further teaches the boot image storing device is a non-volatile memory device (Iga: see for example, Column 1 Line 45 – 48: ROM is one type of non-volatile memory devices).

As per claim 6, Reneris as modified teaches the claimed invention as described above (see claim 1). Iga further teaches said composition memory is a

BIOS ROM (Basic Input Output System Read Only Memory (Iga: see for example, Column 1 Line 45 – 48).

As per claim 8, Reneris teaches the claimed invention as described above (see claim 7). Reneris teaches saving the device / processor state associated with any given state before powering down (Reneris: see for example, Column 16 Line 55 – 56). However, Reneris does not disclose expressly reading out a boot image from the boot image storing device is accomplished according to an initial state of the main memory.

Iga teaches reading out a boot image from the boot image storing device is accomplished according to an initial state of the main memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Iga within the system of Reneris because (a) Reneris teaches saving the device / processor state in any given state into RAM upon powering down the main power supply (Reneris: see for example, Column 16 Line 55 – 56) and (b) Iga further teaches an improved low cost and fast reboot mechanism by saving the entire boot image code using the existing RAM before powering down (i.e. initial state) instead of using regular low speed boot ROM to speed up the booting process (Iga: see for example, Column 2 Line 24 – 26).

As per claim 9, Reneris as modified teaches the claimed invention as described above (see claim 8). Reneris as modified further teaches reading out a boot image from the boot image storing device is accomplished when the computer is powered down (Reneris: see for example, Column 9 Line 44 – 54) & (Iga: see for example, Column 15 – 22).

As per claim 16, Reneris teaches the claimed invention as described above (see claim 7). Reneris teaches saving the device / processor state associated with any given state before powering down (Reneris: see for example, Column 16 Line 55 – 56). However, Reneris does not disclose expressly the boot image being executed to boot said computer while said boot image resides in said main memory.

Iga teaches the boot image being executed to boot said computer while said boot image resides in said main memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Iga within the system of Reneris because (a) Reneris teaches saving the device / processor state in any given state into RAM upon powering down the main power supply (Reneris: see for example, Column 16 Line 55 – 56) and (b) Iga further teaches an improved low cost and fast reboot mechanism by saving the entire boot image code using the existing RAM before powering down (i.e. initial state) instead of using regular

low speed boot ROM to speed up the booting process (Iga: see for example, Column 2 Line 24 – 26).

As per claim 17, Reneris teaches the claimed invention as described above (see claim 7). Reneris teaches saving the device / processor state associated with any given state before powering down (Reneris: see for example, Column 16 Line 55 – 56). However, Reneris does not disclose expressly said computer being booted without having to read said boot image out of said main memory.

Iga teaches said computer being booted without having to read said boot image out of said main memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line 32 – 36).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Iga within the system of Reneris because (a) Reneris teaches saving the device / processor state in any given state into RAM upon powering down the main power supply (Reneris: see for example, Column 16 Line 55 – 56) and (b) Iga further teaches an improved low cost and fast reboot mechanism by saving the entire boot image code using the existing RAM before powering down (i.e. initial state) instead of using regular low speed boot ROM to speed up the booting process (Iga: see for example, Column 2 Line 24 – 26).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reneris (Patent Number: 5784628), in view of Iga (Patent Number: 6226740), and in view of Oka (Patent Number: 5448741).

As per claim 3, Reneris as modified teaches the claimed invention as described above (see claim 1). Reneris as modified does not disclose expressly the boot image storing device is a hard disk drive.

Oka teaches the boot image storing device is a hard disk drive (Oka: see for example, Column 3 Line 21 – 22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Oka within the system of Reneris as modified because it is a commonly available internal storage device among a plurality of bootstrap devices detachable to the personal computer (Oka: see for example, Column 1 Line 13 – 15).

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iga (Patent Number: 6226740), in view of Reneris (Patent Number: 5784628), and in view of Jeon (Patent Number: 6122734).

As per claim 5, Reneris as modified teaches the claimed invention as described above (see claim 1). Reneris as modified does not disclose expressly the boot image storing device is a compact disk drive.

Jeon teaches:

the boot image storing device is a compact disk drive (Jeon, Column 1 Line 43 – 44).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Jeon within the system of Iga because Jeon teaches providing a CD-ROM disk for both booting and repairing a computer system with only the CD-ROM disk (Jeon: see for example, Column 2 Line 65 – 67).

12. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iga (Patent Number: 6226740), in view of Jeon (Patent Number: 6122734).

As per claim 10, Iga teaches a method for powering on a computer receiving main and auxiliary power, the method comprising the steps of:

providing a central processing unit with an instruction pointer, a main memory storing a boot image by receiving the auxiliary power when the main power is shut off, and a basic input/output system memory setting the instruction pointer (Iga: see for example, Column 4 Line 16 – 22: an instruction pointer must be embodied with a CPU to successfully execute booting the system).

setting the instruction pointer of the central processing unit to a boot image storing region of the main memory; and executing an operating system program by reading out the boot image from the boot image storing region of the main memory (Iga: see for example, Column 4 Line 16 – 22 and Column 4 Line

higher speed RAM relative to lower speed ROM storage device), the processor reads out from a contents of high speed RAM instead of the contents of low speed ROM; as a result, this makes it possible to significantly reduce the boot time (Column 4 Line 32 – 36) – Therefore, the instruction pointer must be incorporated into this booting process in order to successfully execute booting the system).

Iga does not disclose expressly checking initializing steps and faults of the hardware components of the computer.

Jeon teaches checking initializing steps and faults of the hardware components of the computer (Jeon: see for example, Column 1 Line 43 – 44).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Jeon within the system of Iga because Jeon teaches providing a CD-ROM disk for both booting and repairing a computer system with only the CD-ROM disk (Jeon: see for example, Column 2 Line 65 – 67).

As per claim 13, Iga teaches the claimed invention as described above (see claim 11). Iga does not disclose expressly said memory for storing said boot image prior to reading out said boot image being a compact dick read only memory (CD-ROM).

Jeon teaches:

said memory for storing said boot image prior to reading out said boot image being a compact dick read only memory (CD-ROM) (Iga, Column 4 Line 16 – 22 and Jeon, Column 1 Line 43 – 44).

Same rationale of combination applied herein as above in rejecting claim 10.

13. Claims 14, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iga (Patent Number: 6226740), in view of Gharda (Patent Number: 6009520).

As per claim 14, Iga teaches the claimed invention as described above (see claim 11). Iga does not disclose explicitly said boot image is accomplished when said boot image is in a compressed format.

Gharda teaches said boot image is accomplished when said boot image is in a compressed format (Gharda: see for example, Column 6 Line 16 – 21).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Gharda within the system of Iga because Gharda teaches an improved method to speedup the booting process for BIOS to be compressed in a ROM chip and for BIOS routines to be shadowed to system RAM where the routines may be accessed and executed in much higher speeds than is possible running directly from ROM (Gharda: see for example, Column 1 Line 36 – 42).

As per claim 15, Iga as modified teaches the claimed invention as described above (see claim 14). Gharda further teaches decompressing said boot image after said compressed boot image is read out (Gharda: see for example, Column 6 Line 16 – 21).

As per claim 20, Iga teaches the claimed invention as described above (see claim 11). Iga does not disclose explicitly decompressing said boot image after said reading step and before said loading step.

Gharda teaches decompressing said boot image after said reading step and before said loading step (Gharda: see for example, Column 6 Line 16 – 21). Same rationale of combination applied herein as above in rejecting claim 14.

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reneris (Patent Number: 5784628), in view of Iga (Patent Number: 6226740), and in view of Gharda (Patent Number: 6009520).

As per claim 19, teaches the claimed invention as described above (see claim 1). Reneris as modified does not disclose explicitly said boot image being stored in said main memory in decompressed format.

Gharda teaches said boot image being stored in said main memory in decompressed format (Gharda: see for example, Column 6 Line 16 – 21).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Gharda within the

system of Reneris as modified because Gharda teaches an improved method to speedup the booting process for BIOS to be compressed in a ROM chip and for BIOS routines to be shadowed to system RAM where the routines may be accessed and executed in much higher speeds than is possible running directly from ROM (Gharda: see for example, Column 1 Line 36 – 42).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 571-272-3788. The examiner can normally be reached on Monday-Friday 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Longbit Chai
Examiner
Art Unit 2131

LBC

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